

SOI-Multi-fin FET: Number of Fins Influence on Corner Effect

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ABSTRACT

SOI-Multifin-FET was analyzed by a three-dimensional numerical device simulator and its electrical characteristics and potential distribution in the oxide and the silicon in the section perpendicular to the flow of the current were compared for single-fin, three-fin and five-fin FET to investigate the influence of *fin*s number on corner effect in Dual-gate SOI Multi-FinFET, and we provide a comparison with a Tri-gate SOI Multi-FinFET structure.

Keywords: SOI, FinFET, Corner effect, Dual-gate, tri-gate, Multi-Fin FET.

I. INTRODUCTION

Recently, the Dual-gate structure has attracted a great deal of attention for its potential as a technology driver for sub-hundred-nanometer MOSFET. The two gates of a SOI-FinFET can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. Further, SOI-FinFET devices are built utilizing multiple parallel fins between the source and drain which introduces a large total channel width to achieve high transconductance, maintain good noise and mismatch performance¹. Fig.1(a) shows a structure of a multifin FET. This device consists of a thin silicon body,

the thickness of which is denoted by T_{Si} , wrapped by gate electrodes. The current flows parallel to the wafer plane, whereas the channel is formed perpendicular to the plane of the wafer. Due to this reason, the device is termed quasi-planar. The independent control of the front and back gates of the FinFET is achieved by etching away the gate electrode at the top of the channel. The effective gate width of a FinFET is $2nh$, where n is the number of fins and h is the fin height.

Thus, wider transistors with higher on-currents are obtained by using multiple fins. The *fin* pitch (p) is the minimum pitch between adjacent *fin*s allowed by lithography at a particular technology node.

Using spacer lithography, p can be made as small as half of the lithography pitch².

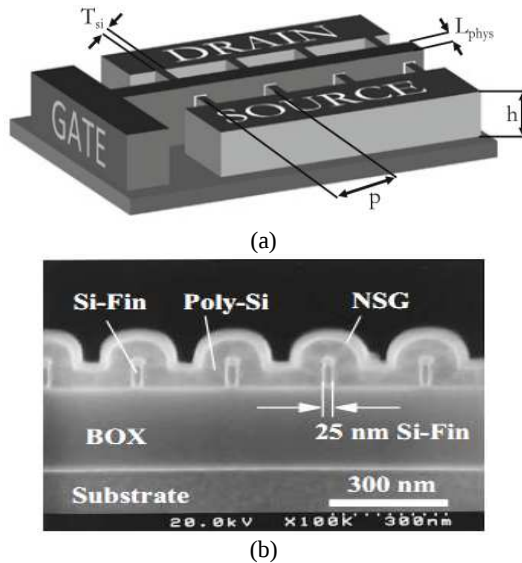


Figure 1: (a) schematic diagram of the multi-Fin structure, (b) Cross-sectional SEM image of the fabricated Multifin-FET with 5-Fins³.

Fig.1(b) shows the cross-sectional SEM image of the fabricated SOI-five-fin-FET. It should be noted that the widths at the top and bottom of the Si-Fin is entirely the same i.e., the Si-Fin shows the ideal rectangular channel shape.

The measured I_d - V_d characteristics of the Multifin-FET with a single-Fin and five-Fins are shown in Fig. 2 (a and b). It is apparent that 5 times of the drain current is accurately obtained in the five-Fin device compared with that of in the single-Fin device at a fixed gate voltage and drain voltage.

The corners present leads to the formation of independent channels with different threshold voltages. This phenomenon is known as corner effect and it needs to be suppressed by additional corner

implantation and/or corner rounding⁴⁻⁵. Corner implantation uses the fin formation hard mask and allows a retarget of Tri-Gate threshold voltage independent of the halo implantation shared with the planar MOSFETs. The radius of curvature of the corners has a significant impact on the device electrical characteristics and can decide whether or not a different threshold voltage will be measured at the corners and at the planar interfaces of the device⁶. So, Corner rounding erases electric field overlapping of Top- and Side-Gate and permits a homogenous transition between Top-and Side-Channel⁵.

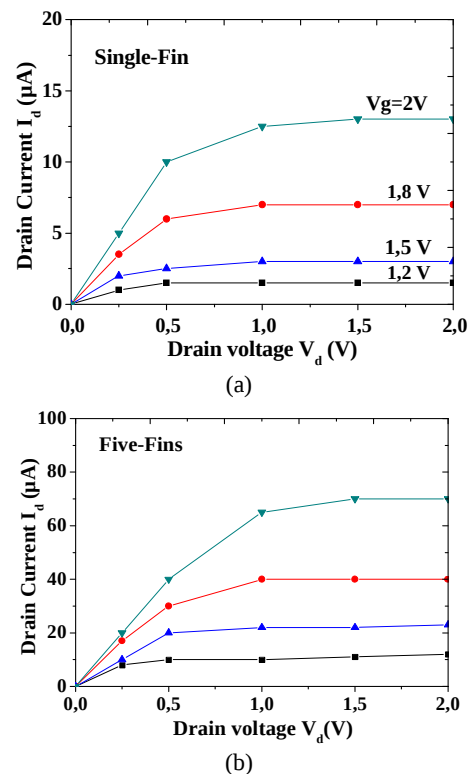


Fig.2. I_d - V_d Characteristics of the fabricated SOI-Multifin FET a) - Single Fin; b) - Five-fin

II. SIMULATION AND RESULTS:

We first optimize a single-finFET which then will be used as a base transistor for a multi-fin structure⁷. The gate length (L_g) of the n-type FinFET is set at 25 nm, the fin height (H_{fin}) is fixed at 40 nm and the fin width (W_{fin}) at 40 nm. The bulk is lightly doped 10^{18} cm^{-3} to avoid the dopant fluctuation.

With extensive calibrated TCAD Silvaco simulations⁸, we present results for a comparison of the potential in the oxide and the silicon in the section perpendicular to the flow of the current for various numbers of *fins* from $n=1$ fin to 3 fins and finally 5 fins

in the case of dual-gate SOI-Multifin FET and we will compare these results with the case of tri-gate SOI-Multifin FET as shown in (fig.3.a.b.c).

For both dual and tri-gate SOI-Five-fins FET potential in silicon is nearly identical in the vertical direction. There is only one small portion of the potential which is not identical in the vertical direction near to the interfaces between the silicon and the gate above silicon and oxide of the substrate and which is smaller in tri-gate SOI-Multifin FET because this last result from the penetration of the influences of side gates through oxide above the silicon and oxide of substrate.

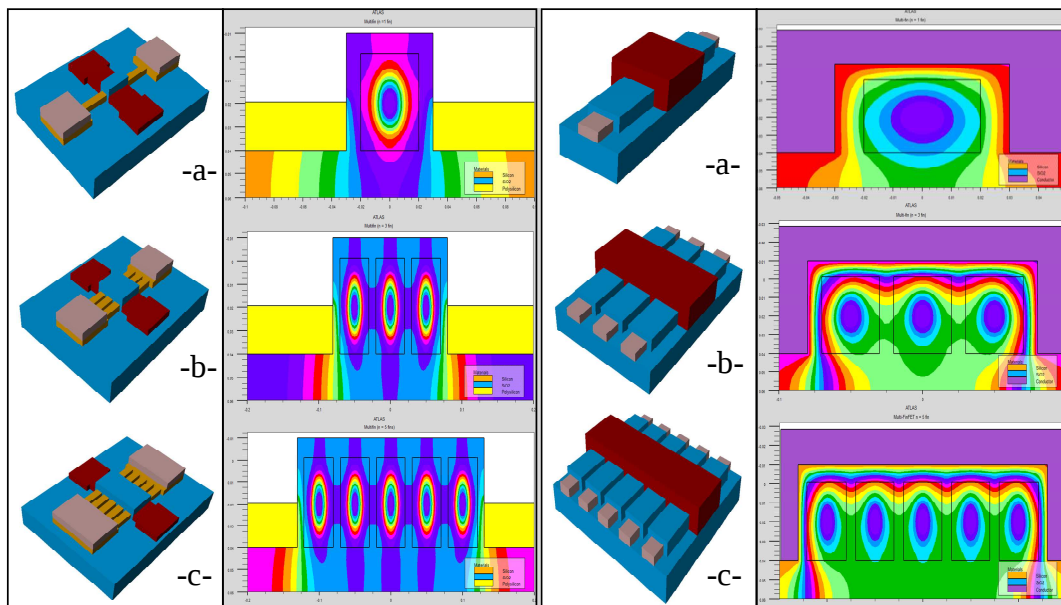


Figure 3: Potential in the oxide and the silicon in the y-z section for the Dual-gate and tri-gate Multifin-FET ($V_{gs}=0.5V$) -a-Single fin -b- Three fins - c-Five fins

The corner effect at negative gate voltages results in a penetration of the negative surface potential into the active silicon and the consequence is the reverse

corner effect, this means the depletion of the leakage current in the corners. The current density is mainly concentrated close to the surface and drops down rapidly. The

enhancement of the current due to corner effect extends only over a very small region near the corner. This is due to a short screening length inside of inversion layer. The major effect in the double gate transistor is the suppression of the current near the upper surface of the fin, the on-current of the double gate transistors is higher than a simple estimation of 2/3 of the current of the triple gate transistors. In fact, the upper part of the fin also contributes to the total current of the open double gate transistor. A slight enhancement of the current in the corners of the fin in the open transistors is observed for both transistors.

CONCLUSION

The higher on-state drain current in case of the SOI FinFET is caused by the corner effect, which is effectively doubled in the SOI FinFET compared to the bulk FinFET.

Since the corners effect is located at each fin, with increasing the fin number the influence of the corner effect became stronger.

In contrast, This effect improves the performance of the FinFETs since the on-current is enhanced at the corners and the leakage current is suppressed. Due to positive influence of the corner effect, the triple gate wrap around design of the SOI-Multifin FET appears to be more advantageous in comparison to the double gate design.

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